What is claimed is:

1. A semiconductor memory device comprising:

a plurality of first connection lines arranged in parallel with each other in a same layer, each connecting to a different contact portion;

a plurality of second connection lines arranged in parallel with each other in the same layer as the first connection lines, the first connection lines and the second connection lines being arranged in an alternating fashion, and each of the second connection lines connecting to a different contact portion;

a plurality of first plugs each formed on one of the first connection lines;

a plurality of second plugs each formed on one of the second connection lines;

a plurality of first metal wiring lines connecting to the first plugs; and

a plurality of second metal wiring lines formed in a layer different from that of the first metal wiring lines, and connecting to the second plugs,

the first metal wiring lines and the second metal wiring lines differing from each other with respect to at least one of thickness and width, and a product of a wiring capacitance between adjacent two of the first metal wiring lines and a wiring resistance of the first metal wiring lines being substantially the same as a product of those of the second metal wiring lines.

2. The semiconductor memory device according to claim 1, wherein the first metal wiring lines and the second metal wiring lines are formed of a same material, and constitute bit lines of a memory cell array.

3. The semiconductor memory device according to claim 2, wherein:

the layer of the first metal wiring lines are located

lower than the layer of the second metal wiring lines; and

a thickness of the first metal wiring lines is thinner than a thickness of the second metal wiring lines.

4. The semiconductor memory device according to claim 3, wherein:

the layer of the second metal wiring lines constitutes a power supply line in a periphery circuit region of the memory cell array.

5. The semiconductor memory device according to claim 3, wherein a thickness of a dielectric film formed between adjacent two of the first metal wiring lines are thinner than a thickness of a dielectric film formed between adjacent two of the second metal wiring lines.

6. The semiconductor memory device according to claim 1, wherein a relative dielectric constant of a dielectric film formed between adjacent two of the first metal wiring lines is different from a relative dielectric constant of a dielectric film formed between adjacent two of the second metal wiring lines.

7. The semiconductor memory device according to claim 1, wherein either or both of the first metal wiring lines and the second metal wiring lines are damascene wiring lines.

8. The semiconductor memory device according to claim 1, wherein:

a memory circuit including a memory cell array and a logic circuit are formed on a same chip; and

the first and second metal wiring lines constitute bit lines of the memory cell array.

9. The semiconductor memory device according to claim 8, wherein the first and second metal wiring lines further

constitute a wiring pattern of the logic circuit.

10. A semiconductor memory device comprising:

a plurality of first connection lines arranged in parallel with each other in a same layer, each connecting to a different contact portion;

a plurality of second connection lines arranged in parallel with each other in the same layer as the first connection lines, the first connection lines and the second connection lines being arranged in an alternating fashion, and each of the second connection lines connecting to a different contact portion;

a plurality of first plugs each formed on one of the first connection lines;

a plurality of second plugs each formed on one of the second connection lines;

a plurality of first metal wiring lines connecting to the first plugs; and

a plurality of second metal wiring lines formed in a layer different from that of the first metal wiring lines, and connecting to the second plugs,

the first metal wiring lines and the second metal wiring lines differing from each other with respect to at least one of material and constitution, and a product of a wiring capacitance between adjacent two of the first metal wiring lines and a wiring resistance of the first metal wiring lines being substantially the same as a product of those of the second metal wiring lines.

11. The semiconductor memory device according to claim 10, wherein the first metal wiring lines and the second metal wiring lines constitute bit lines of a memory cell array.

12. The semiconductor memory device according to claim 10, wherein a relative dielectric constant of a dielectric film formed between adjacent two of the first metal wiring lines

is different from a relative dielectric constant of a dielectric film formed between adjacent two of the second metal wiring lines.

13. The semiconductor memory device according to claim 10, wherein either or both of the first metal wiring lines and the second metal wiring lines are damascene wiring lines.

14. The semiconductor memory device according to claim 10, wherein either or both of the first metal wiring lines and the second metal wiring lines have a multi-layer structure obtained by laminating layers of different materials.

15. The semiconductor memory device according to claim 14, wherein:

the first metal wiring lines and the second metal wiring lines have a same width and a same thickness.

16. The semiconductor memory device according to claim 10, wherein:

the layer of the first metal wiring lines are located lower than the layer of the second metal wiring lines;

the material of the second metal wiring lines has a lower resistivity than the material of the first metal wiring lines; and

a relative dielectric constant of a dielectric film formed between adjacent two of the first metal wiring lines is lower than a relative dielectric constant of a dielectric film formed between adjacent two of the second metal wiring lines.

17. The semiconductor memory device according to claim 11, wherein:

the layer of the first metal wiring lines are located lower than the layer of the second metal wiring lines;

the layer of the second metal wiring lines constitutes

a power supply line in a periphery circuit region of the memory cell array; and

the layer of the first metal wiring lines constitutes a signal line in the periphery circuit region.

18. The semiconductor memory device according to claim 10, wherein:

a memory circuit including a memory cell array and a logic circuit are formed on a same chip; and

the first and second metal wiring lines constitute bit lines of the memory cell array.

19. The semiconductor memory device according to claim 18, wherein the first and second metal wiring lines further constitute a wiring pattern of the logic circuit.

20. The semiconductor memory device according to claim 19, wherein:

the layer of the first metal wiring lines are located lower than the layer of the second metal wiring lines;

the first metal wiring lines are formed of aluminum; and

the second metal wiring lines are formed of copper.